Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-24 and 31 (canceled).

32 (new): A semiconductor device, comprising:

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an active area formed in a semiconductor substrate, wherein said active area comprises nMOS device components including an n-type source region, an n-type drain region, and a gate structure disposed adjacent said active area between said n-type source region and said n-type drain region; and

an isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area, wherein at least a portion of said isolation structure is adapted to modify stresses incurred on said active area, and wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench.

33 (new): The semiconductor device of claim 32, wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

34 (new): A semiconductor device, comprising:

an active area formed in a semiconductor substrate, wherein said active area comprises pMOS device components including a p-type source region, a p-type drain region, and a gate structure disposed adjacent said active area between said p-type source region and said p-type drain region; and

an isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area, wherein said isolation structure comprises a low-modulus, dielectric material disposed within at least a portion of said trench parallel to a channel current direction of the pMOS device components, and wherein said isolation structure comprises a high-modulus, dielectric material disposed within at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

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35 (new): A semiconductor device, comprising:

an active area formed in a semiconductor substrate, wherein said active area comprises pMOS device components including a p-type source region, a p-type drain region, and a gate structure disposed adjacent said active area between said p-type source region and said p-type drain region; and

an isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area, wherein said isolation structure comprises a low-modulus, dielectric material disposed within at least a portion of said trench perpendicular to a channel current direction of the pMOS device components, and wherein said isolation structure comprises a high-modulus, dielectric material disposed within at least a portion of said trench parallel to the channel current direction of the pMOS device components.

36 (new). A semiconductor device, comprising:

an active area formed in a semiconductor substrate, wherein said active area comprises pMOS device components including a p-type source region, a p-type drain region, and a gate structure disposed adjacent said active area between said p-type source region and said p-type drain region; and

an isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area, wherein at least a portion of said isolation structure is adapted to modify stresses incurred on said active area, and wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

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37 (new): The semiconductor device of claim 36, wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the pMOS device components having a depth wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the pMOS device components having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

38 (new): A semiconductor device, comprising:

an active area formed in a semiconductor substrate, wherein said active area comprises pMOS device components including a p-type source region, a p-type drain region, and a gate structure disposed adjacent said active area between said p-type source region and said p-type drain region;

an isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area, wherein at least a portion of said isolation structure is adapted to modify stresses incurred on said active area;

wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the pMOS device components having a depth wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the pMOS device components having a depth

such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5;

and wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

39 (new): A semiconductor device, comprising:

an active area formed in a semiconductor substrate, wherein said active area comprises pMOS device components including a p-type source region, a p-type drain region, and a gate structure disposed adjacent said active area between said p-type source region and said p-type drain region;

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an isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area, and wherein at least a portion of said isolation structure is adapted to modify stresses incurred on said active area;

wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench perpendicular to a channel current direction of the pMOS device components having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5; and

wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

40 (new): A semiconductor device, comprising:

an active area formed in a semiconductor substrate, wherein said active area comprises pMOS device components including a p-type source region, a p-type drain region, and a gate structure disposed adjacent said active area between said p-type source region and said p-type

drain region;

an isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area, and wherein at least a portion of said isolation structure is adapted to modify stresses incurred on said active area;

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wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench perpendicular to a channel current direction of the pMOS device components having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5; and

wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.